REMARKS

I. Summary of Office Action

Claims 1-24 were pending in the above-identified patent application. Claims 11-24 have been withdrawn as being directed to an unelected invention.

Claims 1-10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention.

Claims 1-10 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Claims 1-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Owen et al. U.S. Patent No. 4,876,660 (hereinafter "Owen").

The Abstract was objected to because it contains more than 150 words.

II. Summary of Applicants' Reply

Applicants have amended to Abstract to shorten its length. Applicants have also amended independent claims 1 and 8 to more particularly define the claimed invention. The amendments are fully supported by the application as originally filed, and therefore no new matter has been added.

III. Applicants' Reply to the § 101 Rejection

The Office Action contends that claims 1-10 "merely disclose steps/components for performing multiply-accumulating operation without further disclosing a practical/physical application or a useful and tangible result . . . . ." *See* Office Action, page 4. As such, the Office Action contends that claims 1-10 do not recite statutory subject matter.

Applicants have amended independent claims 1 and 8 to further recite that the result of the accumulate operation is stored for use as an accumulator value. As explained in applicants' specification, applicants' claimed invention advantageously allows for an accumulator value to be initialized or zeroed with minimal latency. *See* specification, ¶¶ 0007 - 0009. As such, applicants submit that independent claims 1 and 8 now recite a useful, concrete, and tangible result -- namely methods for initializing or zeroing an accumulator value with minimal latency. Applicants also submit that the claimed invention is now clearly directed toward statutory subject matter. *See State St. Bank & Trust Co. v. Signature Fin. Group*, 149, F.3d 1368 (Fed. Cir. 1998). Applicants respectfully request, therefore, that the 35 U.S.C. § 101 rejection of claims 1-10 be withdrawn.

IV. Applicants' Reply to the § 112 Rejection

The Office Action also rejected claims 1-10 under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the invention. Namely, the Office Action contends that the limitation "wherein the feedback output is set to zero" is unclear. Applicants have amended each of independent claims 1 and 8 to recite that the feedback output is initially set to zero. The feedback output need not always be set to zero.

Applicants respectfully submit that claims 1-10 now particularly point out and distinctly claim the invention. Applicants respectfully request, therefore, that the 35 U.S.C. § 112, second paragraph, rejection be withdrawn.

V. Applicants' Reply to the § 102 Rejection

The Office Action rejected claims 1-10 as being anticipated by Owen. Owen refers to a fixed-point multiplier-

accumulator architecture. *See* Owen, Abstract. Owen's FIG. 6a shows a functional block diagram of an emmitter-coupled logic (ECL) multiplier-accumulator. *See* Owen col. 7, 47-61; col. 9, ll. 19-61; and FIG. 6A.

The Office Action contends that Owen's FIG. 6A shows each and every claimed feature recited in applicants' independent claims 1 and 8. Applicants respectfully disagree. For example, applicants' independent claim 1 recites that each signal of the first pair of input signals and the feedback output (which is initially set to zero) are concatenated and then this concatenated value is applied to an accumulate operation. The Office Action contends that this claimed feature is met by MUX 32 of Owen's FIG. 6A. Namely, the Office Action contends that "XA and YA are concatenated to form 32-bit into mux 32" (Office Action, page 5). However, MUX 32 in Owen's FIG. 6A does not concatenate any feedback output which is initially set to zero, as recited by independent claim 1. Rather, what the Office Action contends is the feedback output (i.e., a zero input to MUX 56) is fed into MUX 56, and the output of MUX 56 is connected to adder 34. At no point does FIG. 6A show a pair of input signals and a feedback output (which is initially set to zero) concatenated and then applied to an accumulate operation.

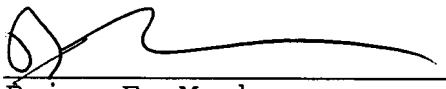
Similarly, applicants' independent claim 8 also recites that the contents of a register are concatenated with the feedback output (which is initially set to zero). As with independent claim 1, the Office Action contends that the feedback output is a zero input to MUX 56. This feedback output, however, is not concatenated with any register value and then applied to an accumulate operation. Rather, registers 14 and 16 are concatenated to form a 32-bit input to MUX 32. *See* Owen, FIG. 6A.

For at least the foregoing reasons, applicants submit that independent claims 1 and 8 are allowable over the prior art of record. Dependent claims 2-7, 9, and 10 are allowable for at least the same reasons. Applicants respectfully request, therefore, that the rejection of claims 1-10 under 35 U.S.C. § 102 be withdrawn.

VI. Conclusion

Applicants respectfully submit that this application, including claims 1-10, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,



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